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(54) Memory controller with a programmable strobe delay

(57) A memory controller is providing that has a clock line (7) for a clock signal; a data bus (2) for connecting to at least one memory module (3, 4, 5); a data latch (6) connected to the data bus (2), for latching data under control of a strobe signal; and a programmable delay (20) for providing the strobe signal in programmed timing relation to the clock signal. The programmable delay comprises, for example, a programmable delay line connected between the clock line (1) and an enabling input (9) of the data latch (6). This arrangement permits the timing of the strobe signal to be adjusted to compensate for changes in memory configuration and other system parameters.

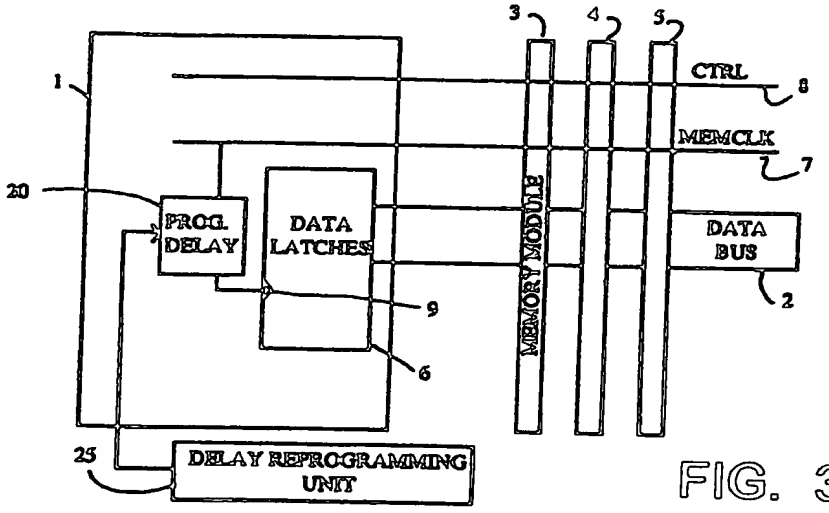

FIG. 3

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Description

Field of the Invention

The present invention relates to a memory controller with a programmable strobe delay. It also relates to a method for programming such a memory controller, and to a method for enhancing the reliability of data reading in a memory controller.

Background of the Invention

The invention addresses the problem of reading data from memories. Figure 1 of the accompanying drawings shows a diagrammatic view of a conventional memory controller 1 together with its associated data bus 2, and several memory modules 3, 4 and 5. The memory controller inter alia comprises a series 6 of data latches connected to the data bus 2. A memory clock signal MEMCLK is present on line 7 in the memory controller 1 and in the different memory modules. The memory controller 1 may transmit on line 8 a control signal CTRL for reading data from the different memory modules, the timing of this signal being related to the clock signal MEMCLK. Data present on the memory bus may be latched in the data latches 6 when an input 9 of the latches is enabled by a strobe signal. The memory address control lines and memory write control lines are not represented in Figure 1.

Figure 2 is a timing diagram of different signals in the device of Figure 1. In Figure 2, 10 is the memory clock MEMCLK signal on line 7. When data is to be read from the memory modules 3, 4, 5, a read signal CTRL 11 is transmitted on line 8. A certain number of memory clock cycles later - say three in the case of Figure 2, the input 9 of the data latches 6 in the memory controller is enabled for latching the data coming from the memory modules 3, 4, 5, which is present on the data bus 2. Reference 12 identifies the strobe signal for enabling the data latches 6, whereas 13, 14, and 15 identify the respective data sent on the data bus 2 by the different memory modules 3, 4, 5. Reference 16 identifies the data window, that is the time period during which the data from the memory modules 3, 4, and 5 may validly be read.

In the Figure 1 system, the delay between the read control signal 11 and the strobe signal enabling the data latches at their input 9 is set by hardware, as shown in Figure 1 by the block 17 between CTRL line 7 and the input 9.

It has also been proposed read data into the latches 6 every clock cycle, the strobe signal being generated at an appropriate time in each clock cycle to ensure proper reading of the data bus. However, the contents of the data latches is only considered valid a predetermined number of MEMCLK clock signal edges after assertion of the CTRL signal as counted by any appropriate circuitry. In this approach, the strobe signal is a clock signal formed by a delayed version of the clock signal MEMCLK, the delay between these two clocks being set, for example, by a conductive path of a given length on the memory-controller circuitboard, between two pins of the memory controller.

The above-described arrangements suffer from several drawbacks. First, they do not address the problem of the effects of changes of configuration in the memory modules, and will therefore not operate for highly loaded and/or very high speed memories. Second, the computation of the strobe-signal delay is a difficult task, and involves numerous experimentations for determining a correct statistical value of the delay.

Summary of the Invention

The present invention addresses the problem of data reading encountered in heavily loaded or high speed memory configurations. This problem arises where the memory bus is highly loaded, e.g. where there are four memory modules or more on the same memory bus; it also arises at high speed, for example 100 MHz or more for the memory clock, for synchronous memory systems. In this case, the difference of transmission time between the memory modules cannot be neglected: the data window 16 (see Figure 1) for reading the data may become fairly small, and even too small for ensuring correct reading of the data in all possible configurations.

Indeed, the data from each memory module may be read for a duration which is typically around 4 or 5 ns for a clock frequency of 125 MHz, and the data window 16 may get reduced by the various skews in the system.

Moreover, the invention addresses the problem arising from the fact that the position and duration of the data window 16 may depend on the actual load on the memory bus 2, which itself depends on the actual configuration of the memory modules. This configuration is not fixed, and may vary at any time according to the user's wish. These problems make it very difficult to design a memory controller that can run at full speed and reliably latch data whatever the memory configuration.

The present invention provides a solution to the problem of providing a memory controller that may run at full speed reliably in any memory configuration, whatever the load on the memory bus and the actual configuration of the memory controller, and even for very high speeds.

According to one aspect of the invention, there is provided a memory controller comprising:

- a clock line for a clock signal;
- data receiving means for connecting to at least one memory module;
- data latching means connected to the data receiving means, for latching data under control of a strobe signal; and

-- programmable means for providing the strobe signal in programmed timing relation to the clock signal.

In one embodiment, the programmable means comprise a programmable delay operatively connected between the clock line and the data latching means. In another embodiment, the programmable means comprise a programmable delay operatively connected between a memory-control line and the data latching means, the memory control line serving to carry a memory-read signal produced in timed relation to the clock signal.

Preferably, delay-programming means are provided for automatically programming the programmable means for providing the strobe signal, the programming means being operative to effect this programming, for example, upon power up of the system including the memory controller.

Advantageously, there are also provided in the system incorporating the memory controller:

-- first means for periodically measuring the value of a parameter indicative of the signal delay characteristics in the system in order to detect variations therein, and
-- second means responsive to variations in said signal delay characteristics detected by the first means, to incrementally change the programming of the programmable means to compensate said programmed timing relation for said variations.

According to another aspect of the present invention, there is also provided a method for programming the programmable means in such a memory controller, the method comprising the steps of:

(a) - programming the programmable means to a given value;
(b) - using the memory controller to write data into memory means;
(c) - using the memory controller to read the data written into the memory means;
(d) - determining whether the data read in step (b) are identical to the data written in step (c);
(e) - repeating steps (a) to (d) until step (d) gives a positive result for at least one given value.
(f) - programming the programmable means to one of said at least one given value.

Step (e) may comprise incrementing the given value, and in this case, once step (d) has given a positive result, steps (a) to (d) are repeated until step (d) gives a negative result.

Alternatively, step (e) may comprise decrementing the given value, and in this case, once step (d) has given a positive result, steps (a) to (d) are repeated until step (d) gives a negative result.

In both cases, step (f) preferably comprises chosing a value among a range of values for which step (d) gives a positive result.

It is also possible that step (e) is repeated for all possible programmable values. In this case, step (f) may comprise:

(g) determining ranges of values for which step (d) gives a positive result;
(h) determining the largest of these ranges of values;

the programmable means being programmed to a value comprised in the largest of said ranges.

According to a further aspect of the present invention, there is provided a method for enhancing the reliability of data reading in a memory controller, comprising programming a delay between a clock signal and a reading strobe signal. This programming can be carried out at power-on of the memory controller.

Brief Description of the Drawings

A memory controller embodying the invention will now be described, by way of non-limiting example, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic view of a conventional memory controller together with several memory modules;
Figure 2 is a timing diagram of different signals in the device of Figure 1;
Figure 3 is a diagrammatic view of a memory controller embodying the invention together with several memory modules;
Figure 4 is a flow chart of a method for programing the strobe signal delay in accordance with the invention.
Figure 5 shows a flowchart of another method for programming the strobe signal delay in accordance with the invention.

Best Mode of Carrying Out the Invention

Figure 3 shows a diagrammatic view of a memory controller 19 embodying the invention together with several memory modules. The memory controller 19 of Figure 3 comprises data latches 6 for latching the data coming from the memory modules 3, 4, and 5 on the data bus 2; these memory modules may for instance be comprised of SDRAM modules. The data latches 6 are enabled by a strobe signal on an input 9. A memory clock signal MEMCLK is present on a clock line 7. In the same general manner described above in relation to the prior art, the strobe signal causes data to be read into the latches 6 every clock cycle, this data being only treated as valid a predetermined number of MEMCLK cycles after assertion of the CTRL signal.

In accordance with the present invention the memory controller 19 comprises programmable means 20 for producing the strobe signal in a programmed timing relation to the clock signal MEMCLK. These programmable means can be used for programming the strobe delay according to the memory configuration, so as to ensure correct data reading relative to the CTRL signal (it being possible to time the strobe signal from the MEMCLK signal because the memory data read signal CTRL is also timed from the MEMCLK signal). As shown in Figure 3, the means 20 may for instance comprise a programmable delay line connected between the memory clock line 7 and the enabling input 9 of the data latches 6. This programmable delay line may comprise a programmable register that determines the delay duration in known manner. This makes the programming of the strobe delay easy to implement, through a simple software programming of one register of the memory controller.

The range and granularity of the strobe delay may depend on the implementation. As an example, a range of 2 to 10 nanoseconds, and a granularity of 150 picoseconds were found to be sufficient for a memory controller accessing up to 4 memory SDRAM modules, at a clock frequency of 125 MHz. If the programmable means 20 comprise a register of the memory controller the size of this register is determined by the range and granularity of the strobe delay.

Figure 3 only shows the components of the memory controller necessary for the understanding of the present invention. The other components of the memory controller 19 are not represented. For instance in the present embodiment the memory controller will include circuitry for enabling reading of the data latches 6 only a predetermined number of MEMCLK cycles after assertion of the CTRL and this circuitry is not represented in Figure 3.

Of course, it would also be possible to implement the present invention in a memory controller of the Figure 1 form by deriving the strobe signal from the control signal CTRL using a programmable delay line. Because the CTRL signal is timed from the MEMCLK signal, this embodiment like that of Figure 3, times the strobe signal relative to the MEMCLK signal though in this case indirectly.

Whichever implementation is used, the memory controllers embodying this invention allow programming of the strobe signal delay according to the circumstances, for instance according to memory modules configuration, according to memory load, and so on. It allows the memory controller to run at full speed reliably in any memory configuration, notwithstanding variations in load on the memory bus and the actual configuration of the memory controller.

As regards the programming of the strobe signal delay into the programmable means, this may be done whenever necessary. In a preferred embodiment of the invention, the means 20 for deriving the strobe signal are programmed by a delay-programming functional block or unit 25 at power-on of the memory controller, to ensure that any change in the memory configuration is properly taken into account. It is also possible to proceed with the programming whenever a change of the memory configuration is detected. The unit 25 for programming the programmable means 20 may take the form of dedicated hardware circuitry provided internally or externally of the memory controller or by a system microprocessor operating under firmware control.

Figure 4 is a flow chart of a method for programming the strobe signal delay in accordance with the invention. The method of Figure 4 is a simple and quick method for programming the means 20 for deriving the strobe signal. In the method of Figure 4, it is assumed that the means 20 for deriving the strobe signal can be programmed to set a delay Δ between the memory clock signal and the strobe signal. The delay Δ may be programmed in a range Δ_{min}-Δ_{max}, with a granularity of g.

In steps 30-42, the program determines a lowest value $\Delta\_$ ensuring a correct reading of the data from the memory.

In step 30, the delay Δ is set to the minimum value Δ_{min}. The program proceeds to step 31.

In step 31, data is written into the memory. The program proceeds to step 32.

In step 32, data is read from the memory. The program proceeds to step 33.

In step 33, the data read from the memory is compared to the data written into the memory. If the data read and written are different, the program proceeds to step 34. If the data read and written are not different, the program proceeds to step 35.

In step 34, the delay is incremented by g. The program then proceeds to step 31.

By step 35, Δ has a value which has already produced one correct reading of the data in the memory. Preferably, this value is checked in steps 36-41 to ensure that this value of Δ gives correct reading of data for more than one operation. This reliability test is not compulsory, and may be skipped. In this case, the program proceeds directly to step 42.

In steps 36-41, the reliability of the write/read operation with the current value of Δ is checked, by performing i_{max} write and read operations. In step 36, a parameter i is set at 1. The program proceeds to step 37.

In step 37, data is written into the memory. The program proceeds to step 38.

In step 38, data is read from the memory. The program proceeds to step 39.

In step 39, the data read from the memory is compared to the data written into the memory. If the data read and written are different, it is determined that the current value of Δ is not reliable; the program proceeds to step 34. If the data read and written are the same, the program proceeds to step 40.

In step 40, it is checked whether i_{max} write and read

operations have been performed, that is whether $i >= i_{max}$. If this is not the case, the program proceeds to step 41. If this is the case, the current value of Δ has proved reliable for i_{max} +1 write and read operations. The program then proceeds to step 42.

In step 41, i is incremented by 1. The program then proceeds to step 37.

In step 42, the current value of Δ is stored as Δ_-; this value of Δ is the lowest value for which the reading of the data is successful. The value of Δ is then incremented by g. The program then proceeds to step 43.

In steps 43-49 the program determines a value Δ_+ for the delay. In the range from Δ_- to Δ_+, data may be read correctly from the memory.

In step 43, data is written into the memory. The program proceeds to step 44.

In step 44, data is read from the memory. The program proceeds to step 45.

In step 45, the data read from the memory is compared to the data written into the memory. If the data read and written are identical, the program proceeds to step 46. If the data read and written are different, the program proceeds to step 48.

In step 46, it has been determined that the current value of Δ is still resulting in at least one correct reading of the data from the memory. It is possible, optionally, to check whether the current value of Δ ensures correct reading for more that one write/read operation. This may be done using program steps similar to steps 36-41: however, this reliability test is not compulsory, and may be skipped. The current value of Δ is then compared to the maximum value Δ_{max}. If $\Delta = \Delta_{max}$, the prgram proceeds to step 49; else, the program proceeds to step 47.

In step 47, the delay Δ is incremented by g. The program proceeds to step 43.

In step 48, a value of Δ giving at least one incorrect reading of the data in the memory has been reached. At that step it has been determined that values of Δ between Δ_- and Δ - g, i.e. the current value of Δ minus one increment ensure correct reading in the memory. The value Δ - g is stored as Δ_+. The program then proceeds to step 50.

In step 49, it has been determined that the values of Δ between Δ_- and Δ_{max} result in a correct reading of the data in the memory. The value Δmax is stored as Δ_+. The program then proceeds to step 50.

By step 50, it has been ascertained that values of Δ between Δ_- and Δ_+ result in correct reading of the data. The delay Δ may then be programmed at any value within this range, e.g. at the value nearest to $(\Delta_+ - \Delta_-)/2$.

The method of Figure 4 allows for a simple and quick setting of the delay Δ. Other methods are possible; the method of Figure 4 may also be modified. For instance, in the flow chart of Figure 4, each reading step follows a writing step; the information which is written into the memory may vary for each write/read operation, to ensure correct statistical check of the memory; however, it would also be possible to have only one writing step, and to read always the same data. It is also possible to start by determining Δ_+, and then determine Δ_-, the necessary changes being obvious for the person skilled in the art.

In a preferred embodiment of the invention, the whole range of delay values is checked to ascertain whether there exist several appropriate reading windows $[\Delta_-; \Delta_+]$; if this is the case, a value of Δ in the largest window is preferably chosen. Figure 5 shows a flowchart for this method.

In the first step 60, the delay Δ is set to the minimum value Δ_{min}. A parameter j is set to 1. The program proceeds to step 61.

In step 61, a reading range or window $[\Delta_-; \Delta_+]$ is determined, e.g. using steps 31-49 of Figure 4. The program proceeds to step 62.

In step 62, the current values of Δ_- and Δ_+ are stored as Δ_j and Δ_{+j}. The program then proceeds to step 63.

In step 63, Δ_+ is compared to Δ_{max}. If Δ_+ is equal to Δ_{max}, there cannot be any further appropriate window. In this case, the program proceeds to step 65. If this is not the case, the program proceeds to step 64.

In step 64, j is incremented by one, and Δ is incremented by g. The program then proceeds to step 61.

In step 65, for all possible values of j, the difference $\Delta_{+j} - \Delta_j$ is computed. The largest difference is determined. This provides the largest reading window. The program then proceeds to step 66.

In step 66, delay Δ is programmed at any value within this largest reading window, e.g. at the value nearest to $(\Delta_{+j} - \Delta_{-j})/2$, j being the index of the largest reading window, as determined in step 65.

The method of Figure 5 ensures that the value for the delay is chosen in the largest possible range appropriate for reading data from the memory.

The description of the best mode of carrying out the invention was only given as an example. Other embodiments of the invention can be used; for instance, a method other than the one depicted in Figure 4 may be used for programming the strobe signal delay. It is possible to use programming means 20 other than a register in the memory controller, if other suitable programming capabilities are provided.

In addition to programming in a particular value for the strobe signal delay at predetermined points during system operation, the delay-programming unit 25 can be arranged to incrementally adjust the programmed delay value in dependence on variations in supply voltage and/or temperature whereby to compensate for any undesired drifting of the strobe signal during use of the memory controller.

This can be implemented by using a circuit for measuring the value of a parameter sensitive to the signal delay characteristics in the memory subsystem. By way of example, the measured parameter could be the

number of inverters in a chain of inverters needed to produce a predetermined signal delay. The unit 25 further comprises means responsive to changes in the measured parameter value over time to determine an appropriate change in the delay set into the programmable delay 20; these means could take the form of a look-up table. Once an appropriate change in delay has been determined, the unit 25 changes the programmed delay by the appropriate amount.

Although the simplest way of producing the strobe signal is to delay either the MEMCLK or CTRL signal as described above, it will be appreciated that other ways are possible. For example, a separate clock circuit could be used to generate the strobe signal, this clock circuit being synchronised with the MEMCLK signal in a desired phase relation thereto by a suitable phase-locked loop.

Claims

1. A memory controller comprising:

   -- a clock line (7) for a clock signal;
   -- data receiving means (2) for connecting to at least one memory module (3, 4, 5);
   -- data latching means (6) connected to the data receiving means (2), for latching data under control of a strobe signal; and
   -- programmable means (20) for providing said strobe signal in programmed timing relation to said clock signal.

2. A memory controller according to claim 1, wherein the programmable means (20) comprise a programmable delay operatively connected between said clock line (7) and said data latching means (6).

3. A memory controller according to claim 1, further comprising:

   -- a memory control line (8) for a memory-read signal, and
   -- means for producing said memory-read signal in timed relation to said clock signal;

   said programmable means (20) being a programmable delay operatively connected between said memory-control line and said data latching means.

4. A memory controller according to any one of the preceding claims, wherein the programmable means (20) comprise a programmable register for setting said programmed timing relation.

5. A system having at least one memory module, and a memory controller according to claim 1; said system including delay-programming means for automatically programming the programmable means for providing the strobe signal.

6. A system according to claim 5, wherein said programming means effects said programming upon power up of said system.

7. A system having at least one memory module and a memory controller according to claim 1; said system including:

   -- first means for periodically measuring the value of a parameter indicative of the signal delay characteristics in the system in order to detect variations therein, and
   -- second means responsive to variations in said signal delay characteristics detected by said first means, to incrementally change the programming of said programmable means to compensate said programmed timing relation for said variations.

8. A method for programming the programmable means in a memory controller according to claim 1; said method, comprising the steps of:

   (a) - programming the programmable means to a given value;
   (b) - using the memory controller to write data into memory means;
   (c) - using the memory controller to read the data written into the memory means;
   (d) - determining whether the data read in step (b) are identical to the data written in step (c);
   (e) - repeating steps (a) to (d) until step (d) gives a positive result for at least one given value.
   (f) - programming the programmable means to one of said at least one given value.

9. A method according to claim 8, wherein step (e) comprises incrementing said given value, and wherein, once step (d) has given a positive result, steps (a) to (d) are repeated until step (d) gives a negative result.

10. A method according to claim 8, wherein step (e) comprises decrementing said given value, and wherein, once step (d) has given a positive result, steps (a) to (d) are repeated until step (d) gives a negative result.

11. A method according to claim 9 or 10, wherein step (f) comprises chosing a value among a range of values for which step (d) gives a positive result.

12. A method according to claim 8, wherein step (e) is repeated for all possible programmable values.

13. A method according to claim 12, wherein step (f) comprises:

(g) determining ranges of values for which step (d) gives a positive result;
(h) determining the largest of these ranges of values;

and wherein the programmable means are programmed to a value comprised in the largest of said ranges.

14. A method for enhancing the reliability of data reading in a memory controller, comprising programming a delay between a clock signal (10) and a reading strobe signal.

15. A method according to claim 14, wherein said programming is carried out at power-on of the memory controller.

16. A method according to claim 14, wherein said programming is carried out to compensate for voltage variations.

17. A method according to claim 14, wherein said programming is carried out to compensate for variations in processing load.

18. A method according to claim 14, wherein said programming is carried out to compensate for temperature variations.

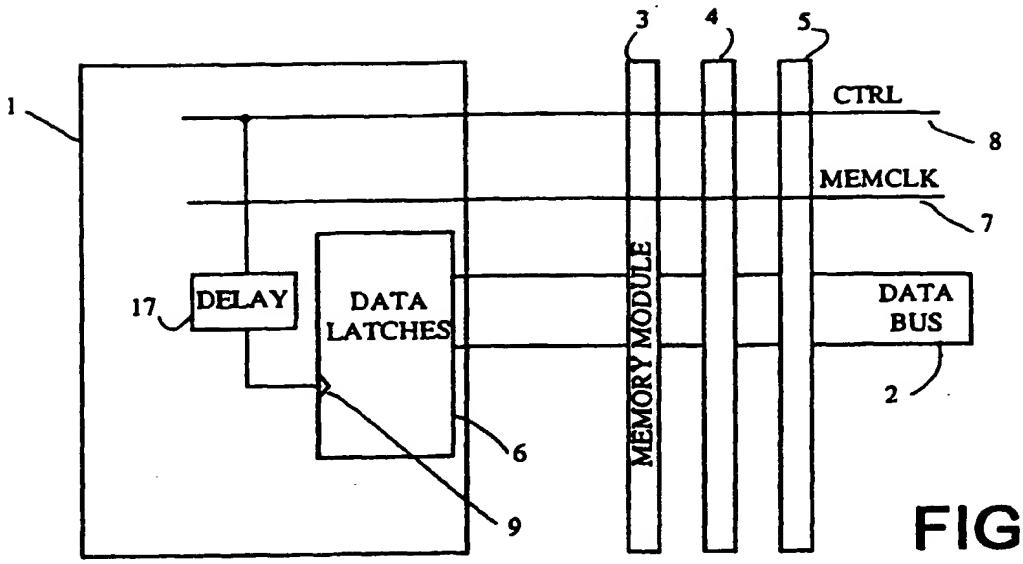
1
3
4
5
CTRL
8
MEMCLK
7
17
DELAY
DATA LATCHES
MEMORY MODULE
DATA BUS
2
6
9

FIG. 1

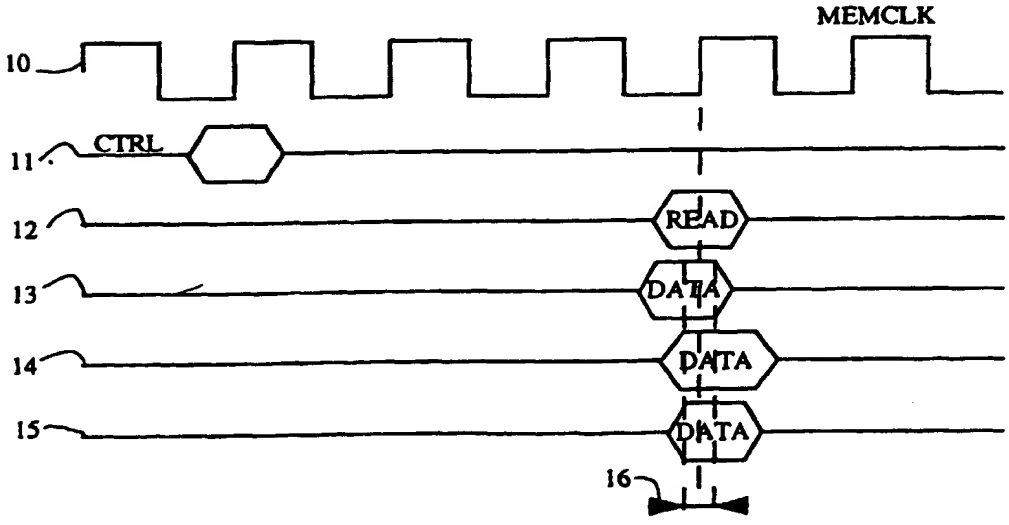
MEMCLK
10
11
CTRL
12
READ
13
DATA
14
DATA
15
DATA
16

FIG. 2

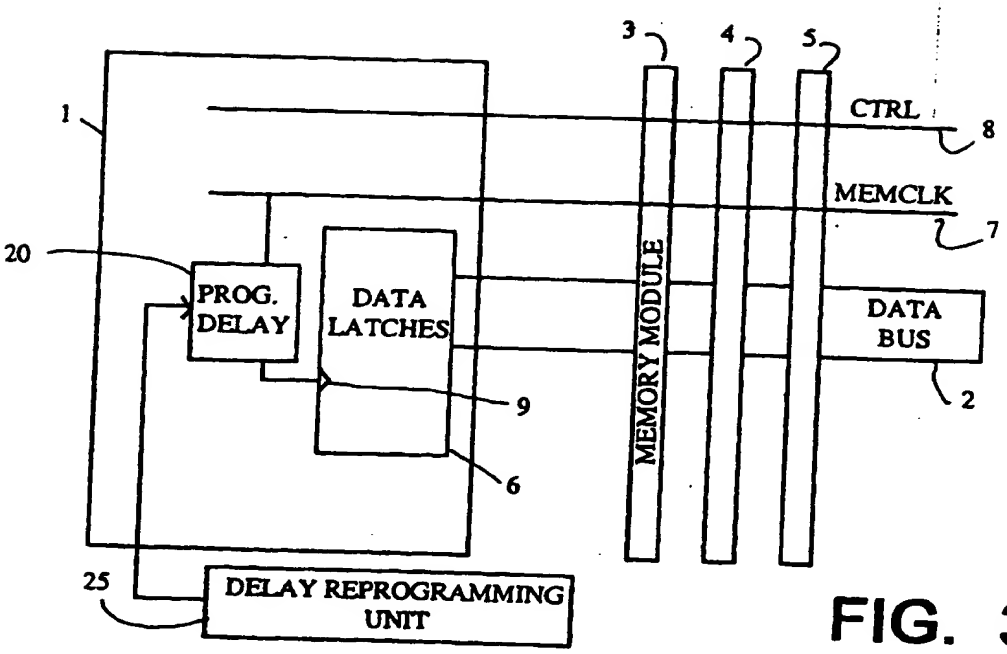
1
3
4
5
CTRL
8
MEMCLK
7
20
PROG. DELAY
DATA LATCHES
MEMORY MODULE
DATA BUS
2
9
6
25
DELAY REPROGRAMMING UNIT

FIG. 3

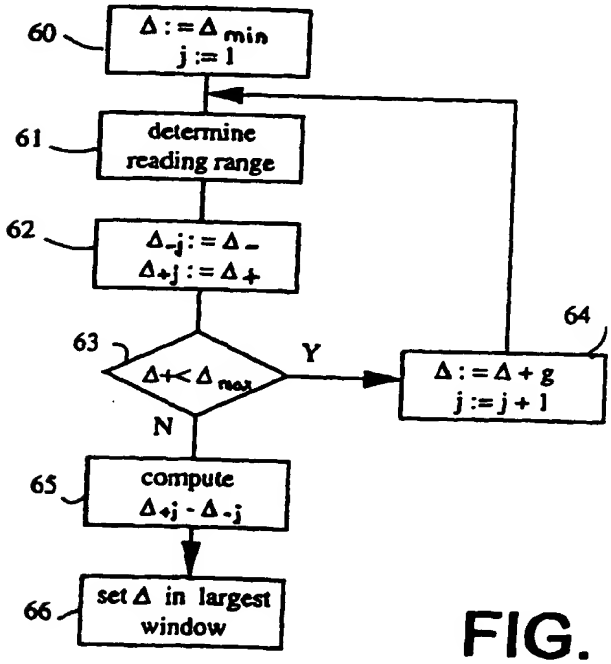
60
Δ := Δ min
j := 1
61
determine reading range
62
Δ-j := Δ-
Δ+j := Δ+
63
Δ+ < Δ neg
Y
64
Δ := Δ + g
j := j + 1
N
65
compute Δ+j - Δ-j
66
set Δ in largest window

FIG. 5

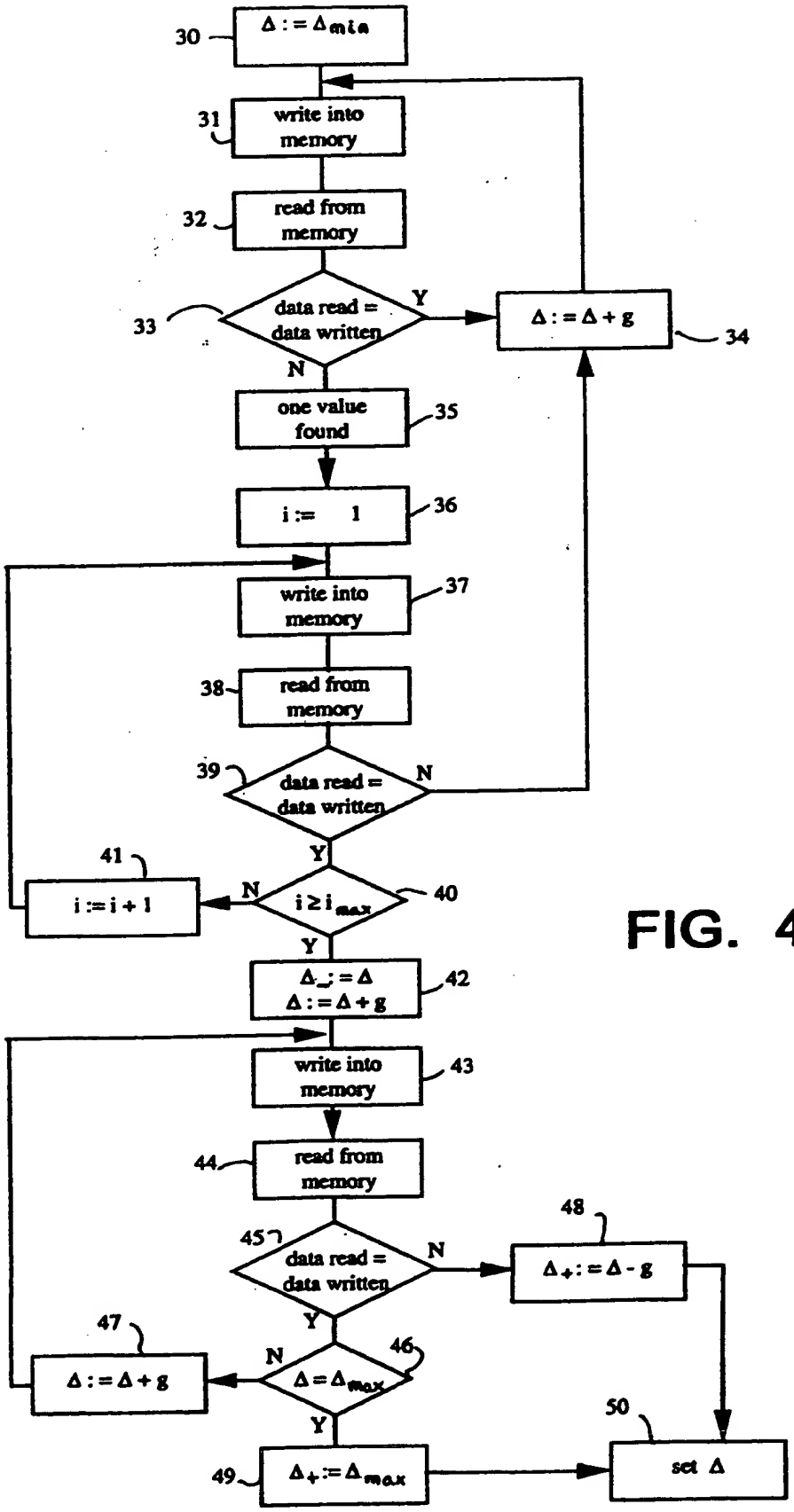
30
Δ := Δmin
31
write into memory
32
read from memory
33
data read = data written
Y
N
Δ := Δ + g
34
one value found
35
i := 1
36
write into memory
37
38
read from memory
39
data read = data written
N
Y
41
i := i + 1
N
i ≥ imax
40
Y
Δ_ := Δ
Δ := Δ + g
42
write into memory
43
44
read from memory
45
data read = data written
N
48
Δ+ := Δ - g
Y
47
Δ := Δ + g
N
Δ = Δmax
46
Y
50
49
Δ+ := Δmax
set Δ

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 41 0009

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	EP 0 379 772 A (DIGITAL EQUIPMENT CORPORATION) * column 2, line 48 - column 3, line 28 * * column 5, line 9 - line 37 * * column 6, line 30 - column 7, line 50 * * column 9, line 8 - line 51 * * figures 1,2 *	1-3,5,7, 14 4,6,15	G06F13/42 G06F13/16
Y	US 5 557 782 A (WITKOWSKI ET AL) * column 2, line 1 - line 18 * * column 5, line 35 - line 63 * * column 6, line 63 - column 7, line 32 * * claims 1-8 *	4,6,15	
A	US 5 560 000 A (VOGLEY) * column 2, line 9 - line 33 * * column 4, line 33 - column 5, line 35 * * claims 1-3 *	1-18	
A	US 5 509 138 A (CASH ET AL) * abstract * * column 2, line 28 - line 63 * * column 14, line 53 - column 15, line 13 *	1-18	TECHNICAL FIELDS SEARCHED (Int.Cl.6) G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 June 1997	McDonagh, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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